9926 JK FLIP-FLOP ELEMENT

TEMPERATURE RANGES —55°C TO +125°C (FULL RANGE)
0°C TO +100°C (MID RANGE)

FAIRCHILD PLANAR* EPITAXIAL MICROLOGIC® INTEGRATED CIRCUITS

JK FLIP-FLOP DESCRIPTION

The Fairchild JK Flip-Flop is a complete, general purpose, storage element suitable for use in shift registers, counters or any type of control function.

The JK Flip-Flop differs from ordinary RS Flip-Flops in that no ambiguous output state can result from simultaneous one inputs. In this JK Flip-Flop simultaneous lows on both the set and clear inputs cause the output state to toggle (reverse). This feature enhances the operation of the JK Flip-Flop in binary counters, as no external feedback connections are required. The toggling action can also be used to advantage for minimizing the logic structure of control units.

The unique input triggering circuit permits the JK Flip-Flop to respond to negative clock pulse transition as short as 1 nanosecond or as long as 100 nanoseconds.

Asynchronous preset and preclear inputs are included for presetting counters, inserting parallel data in registers, and similar applications.

POWER DISSIPATION (25°C) **TYPICAL** 56 mW

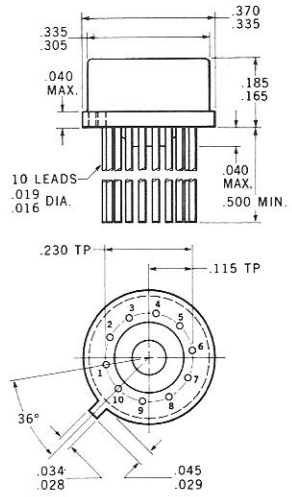
ABSOLUTE MAXIMUM RATINGS (25°C Ambient Temperature)

Maximum Voltage applied to pin 8	+12.0 Volts
Maximum Voltage applied to any input pin	±4.0 Volts
Storage Temperature	-65°C to +150°C
Power Dissipation	500 mW

OPERATING VOLTAGE RANGE

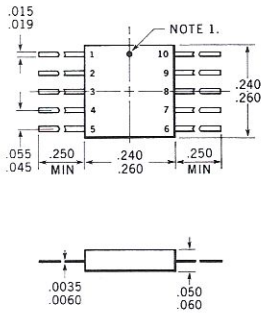
Collector Supply Voltage (V_{CC})	3.0 Volts ±10%

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO—100)



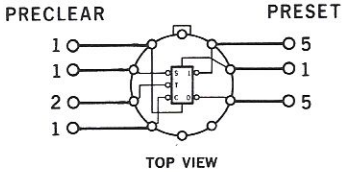
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

CERPAK - FLAT PACKAGE
TOP VIEW



NOTE 1. Alternate marking of dot in upper left hand corner is also acceptable.

LOGIC SYMBOL AND LOAD FACTORS



SET (J) (2)	CLEAR (K) (4)	OUTPUT (9)
t = n		t = n + 1
H	H	X^n
H	L	H
L	H	L
L	L	$\overline{X^n}$

H is more positive than **L**.
X is the output state at time **n**.

* Planar is a patented Fairchild process.

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A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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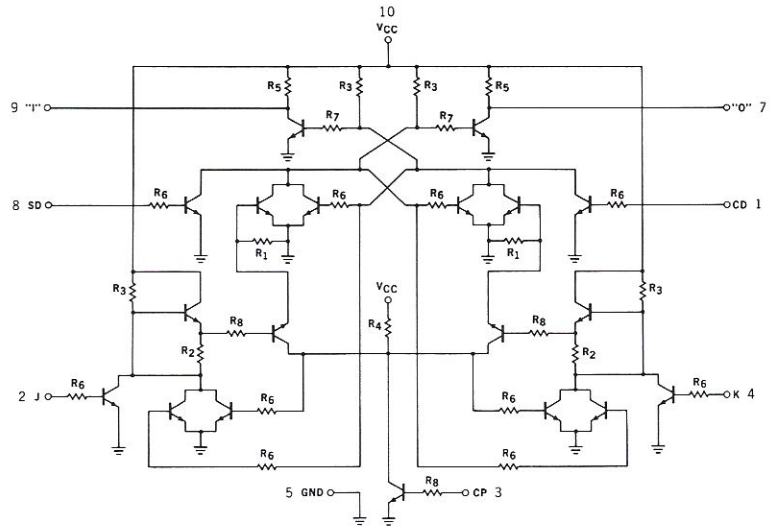
FAIRCHILD MICROLOGIC® I.C. 9926 JK FLIP-FLOP

JK FLIP-FLOP SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 3K\Omega$	$R_5 = 640\Omega$
$R_2 = 1K\Omega$	$R_6 = 600\Omega$
$R_3 = 900\Omega$	$R_7 = 550\Omega$
$R_4 = 700\Omega$	$R_8 = 300\Omega$

Pin configuration for TO-100, cerpak and flatpack are identical.

SWITCHING CHARACTERISTICS (−55°C to +125°C, V_{CC} = 3 V)

Symbol	Characteristic		Minimum	Typical	Maximum
TOGGLING MODE (See Fig. A)					
	Clock Frequency		8 MHz	20	--
	Clock Pulse Duty Cycle at 8 MHz		25%		75%
	Capacitive Load Per Output	(Note 4)			Unlimited
SWITCHING MODE (See Fig. B)					
t_{3-}		(Note 1)	1 ns		200 ns
t_{3-9-} or t_{3-7-}	Lightly Loaded		25 ns	40 ns	50 ns
	Heavily Loaded			45 ns	90 ns
	Heavily Loaded (25°C)	(Note 2)			60 ns
t_{3-9+} or t_{3-7+}	Lightly Loaded		25 ns	35 ns	50 ns
	Heavily Loaded			60 ns	90 ns
	Heavily Loaded (25°C)	(Note 2)			60 ns
t_{2+3-} or t_{4+3-}	(Setup Time)			20 ns	50 ns
t_{2-3-} or t_{4-3-}	(Setup Time			5 ns	30 ns
t_{3-2-} or t_{3-4-}	(Release Time)	(Note 5)		-5 ns	+5 ns
t_{3-2+} or t_{3-4+}	(Release Time)	(Note 5)		-15 ns	0 ns
$t_{1 \text{ or } 8+, \text{ output } -}$	Heavily Loaded			40 ns	90 ns
$t_{1 \text{ or } 8+, \text{ output}+}$	Heavily Loaded	(Note 3)		30 ns	70 ns

NOTES:

(1) Subscripts Denote Respectively: Input Pin, Input Slope, Output Pin, output Slope.

(2) This test is made on all acceptance lots to 4% combined AQL.

(3) If preset or preclear input is high and steering is opposite to preset or preclear, on negative going CP Trigger, the low output will be pulsed high for up to 80 nsec.

(4) Large capacitive loading may limit time of response of output to which capacitance is applied, however, the Flip-Flop will regenerate with any loading.

(5) Release time is defined as the time that the J and K inputs must be maintained after the negative CP transition. Negative release time means the inputs can change momentarily before the CP transition.

FIG. A TOGGLE MODE TEST CIRCUIT

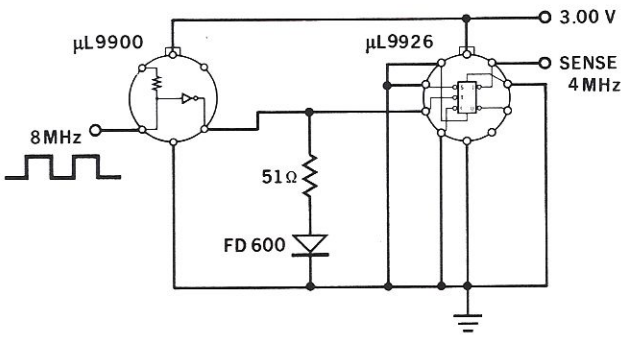
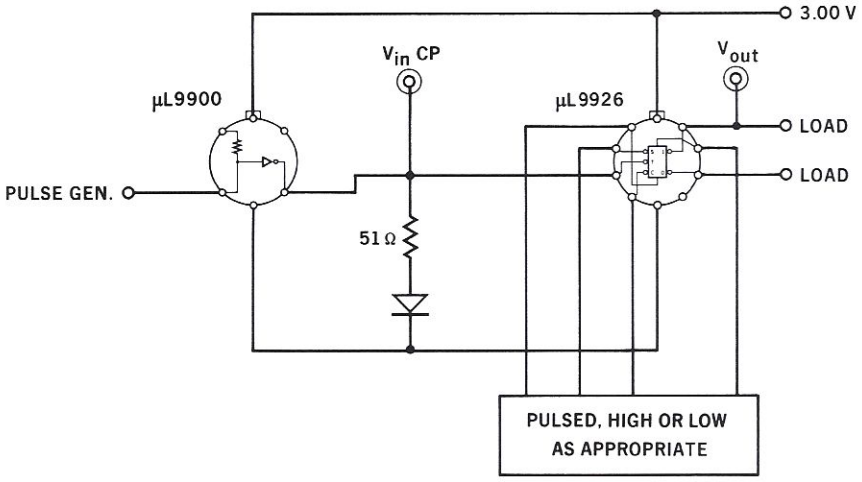
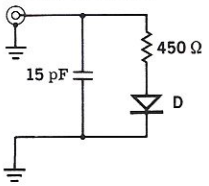


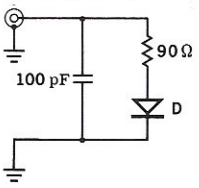
FIG. B SWITCHING MODE TEST CIRCUIT



LIGHTLY LOADED, EACH OUTPUT.

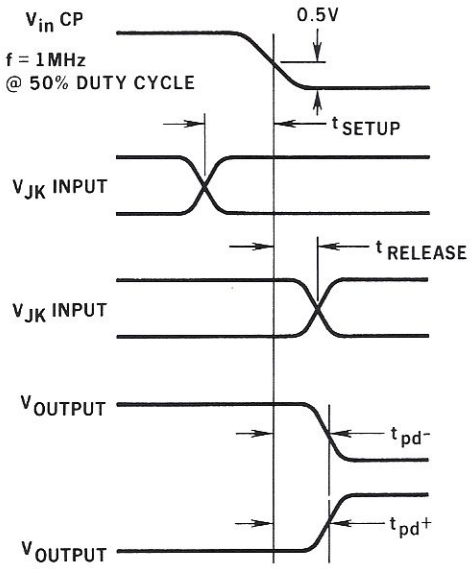


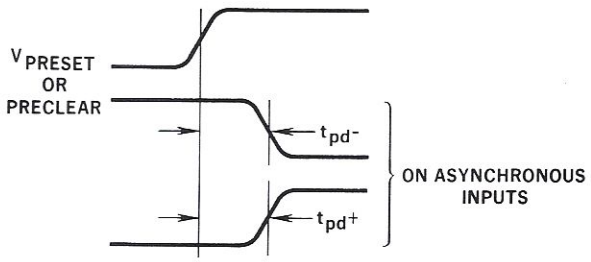
HEAVILY LOADED, EACH OUTPUT.



D = FD600 at temperature of element under test.

Capacitance values include jig and probe.





DC ACCEPTANCE TEST LIMITS FOR FULL-RANGE AND MID-RANGE ELEMENTS

Symbol	Test Tolerance	FULL RANGE -55°C ± 2°C	FULL RANGE 25°C ± 2°C	FULL RANGE +125°C ± 2°C	MID RANGE 0°C ± 2°C	MID RANGE 25°C ± 2°C	MID RANGE 100°C ± 2°C
V_{CC}	± .010 V	3.00 V	3.00 V	3.00 V	3.00 V	3.00 V	3.00 V
V_{IN}	± .002 V	1.014 V	.844 V	.674 V	.909 V	.844 V	.710 V
V_{ON}	± .002 V	1.014 V	.815 V	.674 V	.909 V	.844 V	.710 V
$V_{OD} = V_{BOT}$	± .010 V	1.50 V	1.50 V	1.50 V	1.50 V	1.50 V	1.50 V
V_{OFF}	± .002 V	.710 V	.565 V	.320 V	.574 V	.554 V	.370 V
V_{OUT}		.710 V	.300 V	.320 V	.574 V	.400 V	.370 V
V_{SAT}		.200 V	.210 V	.280 V	.290 V	.260 V	.340 V
I_{IN}		.495 mA	.435 mA	.470 mA	.504 mA	.450 mA	.450 mA
$2I_{IN}$		.990 mA	.870 mA	.940 mA	1.01 mA	.900 mA	.900 mA
I_A		2.47 mA	2.54 mA	2.35 mA	2.52 mA	2.38 mA	2.25 mA

DC ACCEPTANCE TEST CONDITIONS FOR FULL-RANGE AND MID-RANGE ELEMENTS

Test No.	Test Title	Units	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Test Limits Min.	Typ.	Max.
* 1	I_1	mA	V_{IN}				GND					V_{CC}			I_{IN}
2	I_2	mA		V_{IN}			GND			V_{BOT}		V_{CC}			I_{IN}
* 3	I_3	mA		V_{BOT}	V_{IN}	V_{BOT}	GND					V_{CC}			$2I_{IN}$
4	I_4	mA	V_{BOT}			V_{IN}	GND					V_{CC}			I_{IN}
5	I_8	mA					GND			V_{IN}		V_{CC}			I_{IN}
* 6	I_9	mA	V_{ON}				GND			V_{BOT}	V_{ON}	V_{CC}	I_A		
7	I_7	mA	V_{BOT}				GND		V_{ON}	V_{ON}		V_{CC}	I_A		
* 8	V_7	V	V_{ON}				GND			V_{OFF}		V_{CC}			V_{SAT}
9	V_9	V	V_{OFF}				GND			V_{ON}		V_{CC}			V_{SAT}
10	V_7	V		V_{ON}	⌐¬	V_{OFF}	GND			HI		V_{CC}			V_{SAT}
11	V_9	V	HI	V_{OFF}	⌐¬	V_{ON}	GND					V_{CC}			V_{SAT}
12	V_9	V		V_{ON}	⌐¬	V_{ON}	GND			HI		V_{CC}			V_{SAT}
13	V_7	V		V_{OFF}	⌐¬	V_{OFF}	GND			HI		V_{CC}			V_{SAT}
14	V_9	V	HI	V_{OFF}	⌐¬	V_{OFF}	GND					V_{CC}			V_{SAT}
15	V_7	V	HI	V_{ON}	⌐¬	V_{ON}	GND					V_{CC}			V_{SAT}

HI = A momentary application of V_{BOT} before the arrival of the negative going clock pulse.

NOTES:

(A) Purchasing information and Fairchild Assured Customer Test Programs are identical to latest issue Epitaxial μLogic Tentative Specifications.

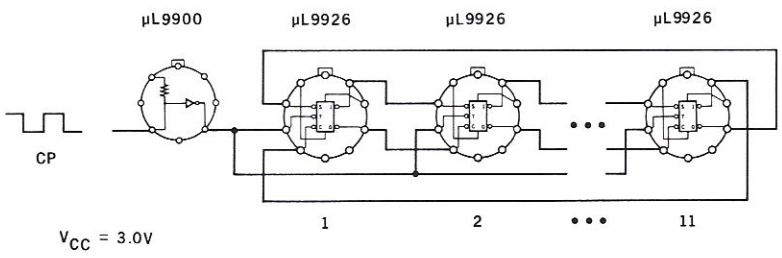
(B) JK926 is available in a TO-100 header with preclear removed and pin connections same as μL916; designated 974.

* FACT program end-point measurement parameter.

FAIRCHILD ASSURED COMPONENT TEST PROGRAM

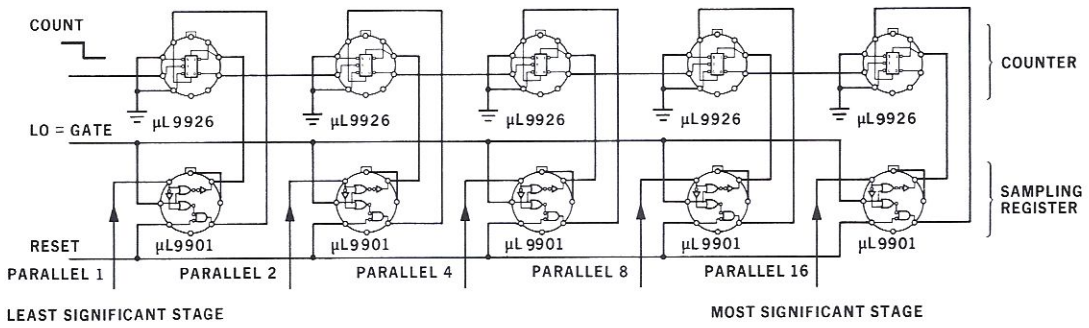
Test No.	25°C	-55 - +125°C	0 - +100°C
1	2a	3a	3a
2	2a	3a	3a
3	2a	3a	3a
4	2a	3a	3a
5	2a	3a	3a
6	2b	3b	3b
7	2b	3b	3b
8	2c	3c	3c
9	2c	3c	3c
10	4		
11	4		
12	4	For definitions refer to	
13	4	the latest FACT brochure.	
14	4		
15	4		

OPERATING LIFE CIRCUIT

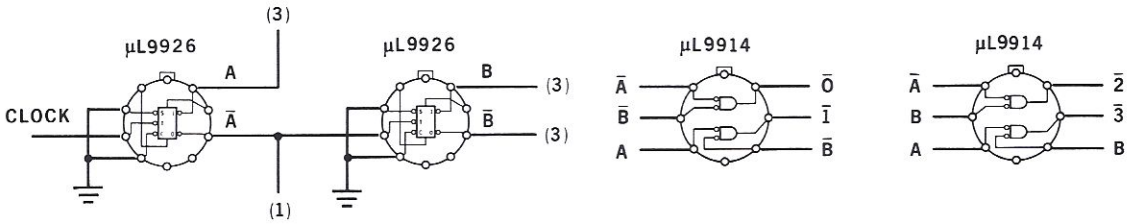


APPLICATIONS

BINARY COUNTER AND SAMPLING CONTROL

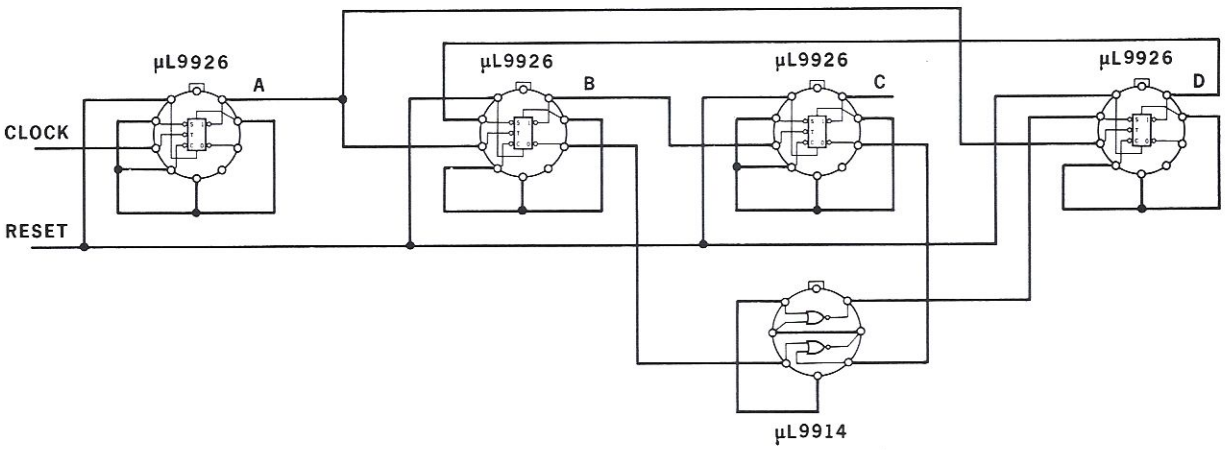


MODULO 4 COUNTER

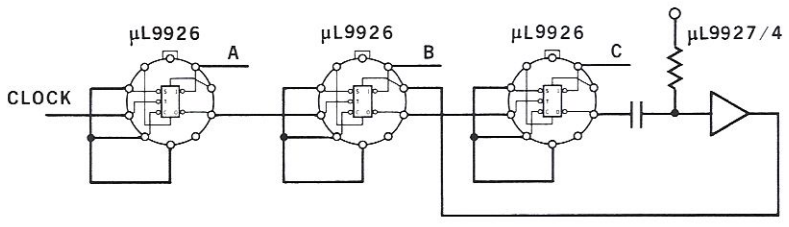


( ) INDICATES REMAINING FAN OUT

1-2-4-8 MODULO 10, COUNT UP COUNTER (POSITIVE LOGIC)



MODULO 6 RIPPLE CARRY



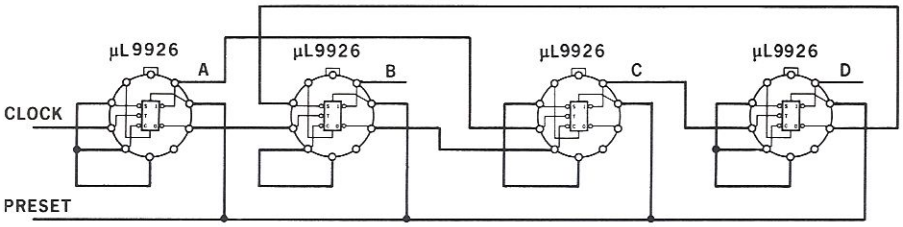
CODE

	A	B	C
0	0	1	0
1	1	1	0
2	0	0	1
3	1	0	1
4	0	1	1
5	1	1	1

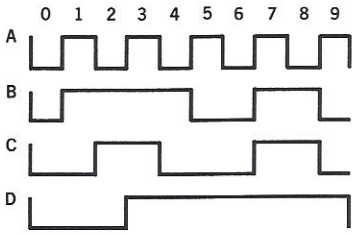
FAIRCHILD MICROLOGIC® I.C. 9926 JK FLIP-FLOP

APPLICATIONS

MODULO 10-MINIMUM HARDWARE

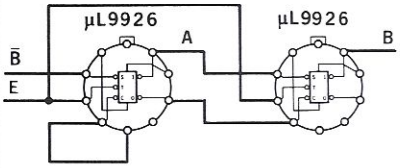


OUTPUT WAVEFORMS



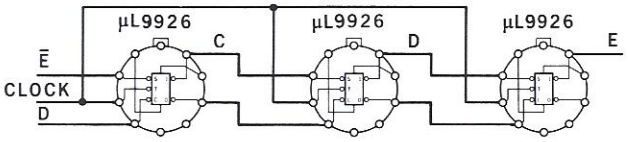
MODULO 15 COUNTER (3x5)

MODULO 3



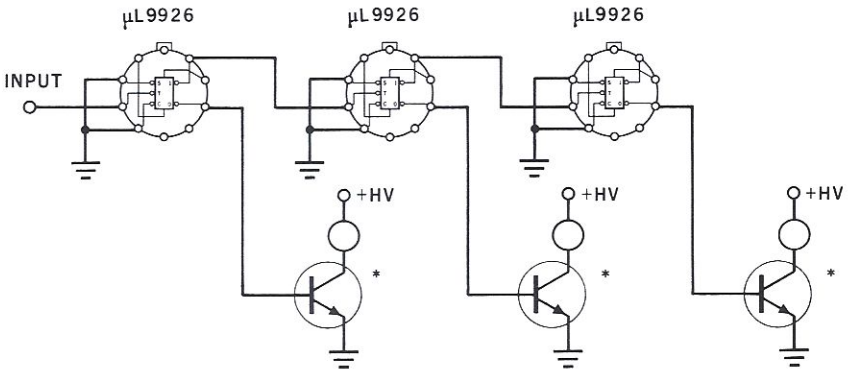
CODE	A	B
0	0	0
1	1	0
2	0	1

MODULO 5



CODE	C	D	E
0	1	0	0
1	1	1	0
2	1	1	1
3	0	1	1
4	0	0	1

BINARY COUNTER, DIRECT READOUT



* 2N2368 INC AND RR COIL, HV ≤ 30VDC
2N1990 NEON AND NIXIE®, HV ≤ 110VDC

NIXIE® - REGISTERED TRADE MARK BURROUGHS CORPORATION.

PURCHASING INFORMATION

To order the 926, the following part numbers should be used to expedite handling.

UA99262BX

A is package designator

A = 3F for ¼ x ¼ Cerpak

A = 5F for Low Profile TO-5

B is operating temperature range designator

B = 1 −55°C to +125°C

B = 2 0°C to +100°C

B = 9 0°C to +70°C

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